

PTO/SB/08A (04-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	
		Filing Date	
		First Named Inventor	Marius Orłowski et al.
		Group Art Unit	
		Examiner Name	
Sheet	1	of	1
		Attorney Docket Number	SC12928TP

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number - Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
JP	AA	US -2003/0040185 A1	02-27-2003	JUN	page 2, [0030] - [0030]
		US -			

FOREIGN PATENT DOCUMENTS						
Examine Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ Number ⁴ Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T. ⁶

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T. ²
JP	AB	MONFRAY et al., "50nm-Gate All Around (GAA) - Silicon On Nothing (SON) - Devices: A Simple Way to Co-Integration of GAA Transistors Within Bulk MOSFET Process," IEEE 2002 Symposium On VLSI Technology Digest of Technical Papers, pp. 108-109.	
JP	AC	BORLAND, "Novel Device Structures by Selective Epitaxial Growth (SEG)," IEEE, 4 pgs. (1987).	
JP	AD	TERADA et al., "A New DRAM Cell with a Transistor on a Lateral Epitaxial Silicon Layer (TOLE Cell)," IEEE Transactions on Electron Devices, Vol. 27, No. 9, September 1990, pp. 2052-2057.	
JP	AE	TERADA et al., "A CMOS/Partial-SOI Structure for Future ULSIs," IEEE SOS/SOT TECHNOLOGY WORKSHOP, p. 37 (1988).	
JP	AF	MONFRAY et al., "SON (Silicon-On-Nothing) P-MOSFETs With Totally Silicided (CoSi ₂) Polysilicon on 5nm-thick Si-films: The Simplest Way to Integration of Metal Gates on Thin FD Channels," IEEE, p. 263-266 (2002).	
JP	AG	MONFRAY et al., "Highly-performant 38nm SON (Silicon-On-Nothing) P-MOSFETs With 9nm-thick Channels," 2002 IEEE International SOI Conference, pp. 20-22.	
JP	AH	MONFRAY et al., "First 80nm SON (Silicon-On-Nothing) MOSFETs With Perfect Morphology and High Electrical Performance," IEEE, pp. 29.7.1-29.7.4 (2001).	
JP	AI	JURCZAK et al., "Silicon-on-Nothing (SON)—an Innovative Process for Advanced CMOS," IEEE Transactions on Electron Devices, Vol. 47, No. 11, November 2000, pp. 2179-2187.	
JP	AJ	BURGHARTZ et al., "Partial-SOI Isolation Structure for Reduced Bipolar Transistor Parasitics," IEEE Electron Device Letters, Vol. 13, No. 8, August 1992, pp. 424-425.	
JP	AK	KUBOTA et al., "A New Soft-Error Immune DRAM Cell With a Transistor On a Lateral Epitaxial Silicon Layer (TOLE Cell)," IEEE, 4 pgs. (1987).	
JP	AL	OGURA, "Partial SOI/SON Formation by He ⁺ Implantation and Annealing," 2002 IEEE International SOI Conference, pp. 185-186.	

Examiner Signature	<i>Rubén J. Maldonado</i>	Date Considered	09/03/2024
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